That which is claimed is:

1. A silicon carbide metal-oxide semiconductor field effect transistor, comprising:

a double implant silicon carbide MOSFET, having an n-type silicon carbide drift layer, spaced apart p-type silicon carbide regions in the n-type silicon carbide drift layer and having n-type silicon carbide regions therein, and a nitrided oxide layer on the n-type silicon carbide drift layer; and

n-type shorting channels extending from respective ones of the n-type silicon carbide regions through the p-type silicon carbide regions and to the n-type silicon carbide drift layer.

2. A silicon carbide metal-oxide semiconductor field effect transistor according to Claim 1, wherein the p-type silicon carbide regions comprise spaced apart regions of silicon carbide having aluminum implanted therein.

3. A silicon carbide metal-oxide semiconductor field effect transistor according to Claim 1, wherein the n-type shorting channels are extend to but not into the n-type silicon carbide drift layer.

4. A silicon carbide metal-oxide semiconductor field effect transistor according to Claim 1, further comprising an epitaxial layer of silicon carbide on the n-type silicon carbide drift layer between the n-type shorting channels.

5. A silicon carbide metal-oxide semiconductor field effect transistor according to Claim 1, further comprising a gate contact on the oxide layer, the gate contact comprising p-type polysilicon.

6. A silicon carbide metal-oxide semiconductor field effect transistor according to Claim 1, wherein the n-type shorting channels are doped so that the n-type channels are self depleted when a zero volt gate bias is applied.

7. A silicon carbide metal-oxide field effect transistor according to Claim 1, further comprising an epitaxial layer of silicon carbide on the n-type silicon carbide

drift layer and the p-type silicon carbide regions and wherein the n-type shorting channels extend into and/or through the epitaxial layer of silicon carbide.

8. A silicon carbide metal-oxide field effect transistor according to Claim 1, wherein the shorting channels have a sheet charge of less than about 10^{13} cm^{-2}.

9. A silicon carbide metal-oxide field effect transistor according to Claim 1, wherein the shorting channels have a sheet charge corresponding to a silicon carbide epitaxial layer having a thickness of about 3500 Å and a carrier concentration of about 2×10^{16} cm^{-3}. $\sim .7 \times 10^{12}$ cm^{-2}

10. A silicon carbide metal-oxide field effect transistor according to Claim 1, wherein the silicon carbide comprises 4H polytype silicon carbide and wherein an interface between the oxide layer and the n-type drift layer has an interface state density of less than 10^{12} $eV^{-1}cm^{-2}$ for energy levels between about 0.3 and about 0.4 eV of a conduction band energy of 4H polytype silicon carbide.

11. A silicon carbide metal-oxide field effect transistor according to Claim 1, wherein the nitride oxide comprises at least one of an oxide-nitride-oxide structure and an oxynitride.

12. A silicon carbide device comprising:

a drift layer of n-type silicon carbide;

first regions of p-type silicon carbide in the drift layer, the first regions of p-type silicon carbide being spaced apart and having peripheral edges which define a region of the drift layer therebetween;

first regions of n-type silicon carbide having a carrier concentration greater than a carrier concentration of the drift layer in the first regions of p-type silicon carbide and spaced apart from the peripheral edges of the first regions of p-type silicon carbide;

second regions of n-type silicon carbide having a carrier concentration less than the carrier concentration of the first regions of n-type silicon carbide and which extend from the first regions of n-type silicon carbide to the peripheral edges of the first regions of p-type silicon carbide; and

a nitrided oxide layer on the drift layer, the first regions of n-type silicon carbide and the second regions of n-type silicon carbide.

13. A silicon carbide device according to Claim 12, wherein the second regions of n-type silicon carbide have a sheet charge of less than about 10^{13} cm^{-2}.

14. A silicon carbide device according to Claim 13, wherein the second regions of n-type silicon carbide have a depth of from about 0.05 μm to about 1 μm.

15. A silicon carbide device according to Claim 14, wherein the second regions of n-type silicon carbide extend a distance of from about 0.5 μm to about 5 μm from the first regions of n-type silicon carbide to the peripheries of the first regions of p-type silicon carbide.

16. A silicon carbide device according to Claim 12, wherein the second regions of n-type silicon carbide have a sheet charge corresponding to a silicon carbide epitaxial layer having a thickness of about 3500 Å and a carrier concentration of about 2×10^{16} cm^{-3}.

17. A silicon carbide device according to Claim 12, wherein an interface state density of an interface between the oxide layer and the drift layer, the first regions of n-type silicon carbide and the second regions of n-type silicon carbide is less than about 10^{12} $eV^{-1}cm^{-2}$ between about 0.3 and about 0.4 eV of the conduction band energy of 4H polytype silicon carbide.

18. A silicon carbide device according to Claim 12, further comprising second regions of p-type silicon carbide disposed in respective ones of the first regions of p-type silicon carbide, wherein the second regions of p-type silicon carbide have a carrier concentration greater than the carrier concentration of the first regions of silicon carbide, the second regions of silicon carbide being adjacent the first regions of n-type silicon carbide and opposite the second regions of n-type silicon carbide.

19. A silicon carbide device according to Claim 12, further comprising a gate contact on the oxide layer.

20. A silicon carbide device according to Claim 19, wherein the gate contact is p-type polysilicon.

21. A silicon carbide device according to Claim 12, wherein the first regions of p-type silicon carbide are spaced apart by a distance of from about 1 μm to about 10 μm.

22. A silicon carbide device according to Claim 21, wherein the first regions of p-type silicon carbide have a carrier concentration of from about 1×10^{16} to about 2×10^{19} cm^{-3}.

23. A silicon carbide device according to Claim 12, further comprising contacts on the first region of p-type silicon carbide and the first region of n-type silicon carbide.

24. A silicon carbide device according to Claim 12, further comprising:

a layer of n-type silicon carbide having a carrier concentration greater than the carrier concentration of the drift layer and disposed adjacent the drift layer opposite the oxide layer; and

a drain contact on the layer of n-type silicon carbide.

26
~~25~~. A silicon carbide device according to Claim 12, further comprising an epitaxial layer of silicon carbide on the first p-type regions and the drift layer of n-type silicon carbide, wherein the second regions of n-type silicon carbide extend into the epitaxial layer, the first regions of n-type silicon carbide extend through the epitaxial layer and the oxide layer is on the epitaxial layer, the first regions of n-type silicon carbide and the second regions of n-type silicon carbide.

27 26
~~26~~. A silicon carbide device according to Claim ~~25~~, wherein the epitaxial layer comprises undoped silicon carbide.

28 26
27. A silicon carbide device according to Claim 25, wherein the epitaxial layer of silicon carbide comprises an epitaxial layer of silicon carbide having a thickness of from about 0.05 μm to about 1 μm.

29 28
28. A silicon carbide device according to Claim 27, wherein the epitaxial layer of silicon carbide comprises an epitaxial layer of silicon carbide having a thickness of from about 1000 to about 5000 Å.

30 26
29. A silicon carbide device according to Claim 25, wherein the epitaxial layer comprises n-type silicon carbide having a sheet charge of less than about 10^{13} cm^{-2}.

31 26
30. A silicon carbide device according to Claim 25, wherein the second regions of n-type silicon carbide have a sheet charge of less than about 10^{13} cm^{-2}.

32 31
31. A silicon carbide device according to Claim 30, wherein the second regions of n-type silicon carbide have a depth of from about 0.05 μm to about 1 μm.

33 32
32. A silicon carbide device according to Claim 31, wherein the second regions of n-type silicon carbide extend a distance of from about 0.5 μm to about 5μm from the first regions of n-type silicon carbide to the peripheries of the first regions of p-type silicon carbide.

34 26
33. A silicon carbide device according to Claim 25, wherein an interface state density of an interface between the oxide layer and the epitaxial layer, the first regions of n-type silicon carbide and the second regions of n-type silicon carbide is less than about 10^{12} $eV^{-1}cm^{-2}$ between about 0.3 and about 0.4 eV of the conduction band energy of 4H polytype silicon carbide.

35 26
34. A silicon carbide device according to Claim 25, further comprising second regions of p-type silicon carbide disposed in respective ones of the first regions of p-type silicon carbide, wherein the second regions of p-type silicon carbide have a carrier concentration greater than the carrier concentration of the first regions of silicon carbide, the second regions of silicon carbide being adjacent the first

regions of n-type silicon carbide and opposite the second regions of n-type silicon carbide.

36 35
~~35~~. A silicon carbide device according to Claim ~~34~~, further comprising:

windows in the epitaxial layer positioned to expose the second regions of p-type silicon carbide; and

first source contacts within the window on the second regions of p-type silicon carbide and on the first regions of n-type silicon carbide.

37 26
~~36~~. A silicon carbide device according to Claim ~~25~~, further comprising a gate contact on the oxide layer.

38 37
~~37~~. A silicon carbide device according to Claim ~~36~~, wherein the gate contact is p-type polysilicon.

39 26
~~38~~. A silicon carbide device according to Claim ~~25~~, wherein the first regions of p-type silicon carbide are spaced apart by a distance of from about 1μm to about 10μm.

40 39
~~39~~. A silicon carbide device according to Claim ~~38~~, wherein the first regions of p-type silicon carbide have a carrier concentration of from about 1×10^{16} to about 2×10^{19} cm^{-3}.

41 26
~~40~~. A silicon carbide device according to Claim ~~25~~, further comprising:

a layer of n-type silicon carbide having a carrier concentration greater than the carrier concentration of the drift layer and disposed adjacent the drift layer opposite the oxide layer; and

a drain contact on the layer of n-type silicon carbide.

25
~~41~~. A silicon carbide metal-oxide field effect transistor according to Claim 12, wherein the nitride oxide layer comprises at least one of an oxide-nitride-oxide structure and an oxynitride layer.

42. A method of fabricating a silicon carbide device, the method comprising:

implanting p-type impurities in a layer of n-type silicon carbide so as to provide first regions of p-type silicon carbide, the first regions of p-type silicon carbide being spaced apart and having peripheral edges which define a region of the layer of n-type silicon carbide therebetween;

implanting n-type impurities into the first regions of p-type silicon carbide to provide first regions of n-type silicon carbide having a carrier concentration greater than a carrier concentration of the layer of silicon carbide, the first regions of n-type silicon carbide being spaced apart from the peripheral edges of the first regions of p-type silicon carbide;

implanting n-type impurities into the first regions of p-type silicon carbide to provide second regions of n-type silicon carbide having a carrier concentration less than the carrier concentration of the first regions of n-type silicon carbide and which extend from the first regions of n-type silicon carbide to the peripheral edges of the first regions of p-type silicon carbide; and

patterning an oxide layer on the drift layer, the first regions of n-type silicon carbide and the second regions of n-type silicon carbide so as to provide a gate oxide.

43. A method according to Claim 42, wherein the steps of implanting p-type impurities, implanting n-type impurities to provide first regions of n-type silicon carbide and implanting n-type impurities to provide second regions of n-type silicon carbide, comprise:

patterning a first mask on the layer of n-type silicon carbide, the first mask having openings corresponding to the first regions of p-type silicon carbide so as to expose portions of the layer of n-type silicon carbide; then

implanting p-type impurities into the layer of n-type silicon carbide utilizing the first mask; then

implanting n-type impurities into the first regions of p-type silicon carbide utilizing the first mask; then

patterning a second mask on the layer of n-type silicon carbide, the second mask having openings corresponding to the first regions of n-type silicon carbide so as to expose portions of the layer of n-type silicon carbide having the p-type and n-type impurities implanted therein; then

implanting n-type impurities into the layer of n-type silicon carbide utilizing the second mask.

44. The method of Claim 43, wherein the step of implanting n-type impurities into the layer of n-type silicon carbide utilizing the first mask is followed by the step of activating the implanted impurities by annealing at a temperature of at least about 1500 °C.

45. The method of Claim 44, wherein the p-type impurities comprise aluminum.

46. The method of Claim 43, wherein the second mask is patterned so that the second regions of n-type silicon carbide extend a distance of from about 0.5 μm to about 5 μm from the first regions of n-type silicon carbide to the peripheries of the first regions of p-type silicon carbide.

47. The method of Claim 42, wherein the step of implanting n-type impurities to provide second regions of n-type silicon carbide, comprises implanting impurities so that the second regions of n-type silicon carbide have a sheet charge of less than about 10^{13} cm^{-2}.

48. The method of Claim 47, wherein the step of implanting n-type impurities to provide second regions of n-type silicon carbide, further comprises implanting n-type impurities utilizing an implant energy so as to provide second regions of n-type silicon carbide have a depth of from about 0.05 μm to about 1 μm.

49. The method of Claim 42, wherein the step of patterning an oxide layer comprises the step of thermally growing an oxide layer.

50. The method of Claim 49 wherein the step of thermally growing an oxide layer comprises the step of thermally growing an oxide layer in an NO or an N_2O environment.

51. The method of Claim 49, wherein the step of thermally growing an oxide layer comprises the step of thermally growing an oxynitride layer.

52. The method of Claim 42, wherein the step of patterning an oxide layer comprises the step of forming an oxide-nitride-oxide (ONO) layer.

53. The method of Claim 42, further comprising the step of annealing the oxide layer in at least one of an NO environment or an N_2O environment.

54. The method of Claim 53, wherein the step of annealing provides an interface state density of an interface between the oxide layer and the drift layer, the first regions of n-type silicon carbide and the second regions of n-type silicon carbide of less than about 10^{12} $eV^{-1}cm^{-2}$ within about 0.4 eV of the conduction band energy of 4H polytype silicon carbide.

55. The method of Claim 42, further comprising implanting p-type impurities into the layer of n-type silicon carbide so as to provide second regions of p-type silicon carbide disposed in respective ones of the first regions of p-type silicon carbide, wherein the second regions of p-type silicon carbide have a carrier concentration greater than the carrier concentration of the first regions of silicon carbide, the second regions of silicon carbide being adjacent the first regions of n-type silicon carbide and opposite the second regions of n-type silicon carbide.

56. The method of Claim 42, further comprising forming a gate contact on the gate oxide layer.

57. The method of Claim 56, wherein step of forming a gate contact comprises the step of patterning p-type polysilicon so as to provide a gate contact on the gate oxide layer.

58. The method of Claim 43, wherein the first mask has openings which are spaced apart by a distance of from about 1 μm to about 10 μm.

59. The method of Claim 42, further comprising:

implanting n-type impurities into a face of the layer of n-type silicon carbide opposite the oxide layer so as to provide a second layer of n-type silicon carbide having a carrier concentration greater than the carrier concentration of the layer of n-type silicon carbide; and

forming a drain contact on the second layer of n-type silicon carbide.

60. The method of Claim 42, wherein the layer of n-type silicon carbide comprises a silicon carbide substrate.

61. The method of Claim 42, wherein the steps of implanting p-type impurities, implanting n-type impurities to provide first regions of n-type silicon carbide and implanting n-type impurities to provide second regions of n-type silicon carbide, comprise:

patterning a first mask on the layer of n-type silicon carbide, the first mask having openings corresponding to the first regions of p-type silicon carbide so as to expose portions of the layer of n-type silicon carbide; then

implanting p-type impurities into the layer of n-type silicon carbide utilizing the first mask; then

annealing the layer of n-type silicon carbide and the first regions of p-type silicon carbide at a temperature of at least about 1500 °C; then

growing an epitaxial layer of silicon carbide on the layer of n-type silicon carbide and the first regions of p-type silicon carbide; then

patterning a second mask on the layer of n-type silicon carbide, the second mask having openings corresponding to the second regions of n-type silicon carbide so as to expose portions of the first regions of p-type silicon carbide;

implanting n-type impurities into the epitaxial layer n-type silicon carbide utilizing the second mask; then

patterning a third mask on the layer of n-type silicon carbide, the third mask having openings corresponding to the first regions of n-type silicon carbide so as to expose portions of the first regions of p-type silicon carbide;

implanting n-type impurities into the first regions of p-type silicon carbide and the epitaxial layer of silicon carbide utilizing the third mask; and

wherein the step of patterning an oxide layer comprises patterning an oxide layer on the epitaxial layer, the first regions of n-type silicon carbide and the second regions of n-type silicon carbide to provide a gate oxide.

62. The method of Claim 61, wherein the step of growing an epitaxial layer of silicon carbide comprises growing an undoped epitaxial layer of silicon carbide.

63. The method of Claim 61, wherein the step of growing an epitaxial layer of silicon carbide comprises growing an epitaxial layer of silicon carbide having a sheet charge of less than about 10^{13} cm^{-2}.

64. The method of Claim 61, wherein the step of growing an epitaxial layer of silicon carbide comprises growing an epitaxial layer of silicon carbide having a thickness of from about 0.05 μm to about 1 μm.

65. The method of Claim 64, wherein the step of growing an epitaxial layer of silicon carbide comprises growing an epitaxial layer of silicon carbide having a thickness of from about 1000 to about 5000 Å.

66. The method of Claim 61, wherein the p-type impurities comprise aluminum.

66. The method of Claim 61, wherein the third mask is patterned so that the second regions of n-type silicon carbide extend a distance of from about 0.5 μm to about 5 μm from the first regions of n-type silicon carbide to the peripheries of the first regions of p-type silicon carbide.

68. The method of Claim 61, wherein the step of implanting n-type impurities to provide second regions of n-type silicon carbide, comprises implanting impurities so that the second regions of n-type silicon carbide have a sheet charge of less than about 10^{13} cm^{-2}.

69. The method of Claim 68, wherein the step of implanting n-type impurities to provide second regions of n-type silicon carbide, further comprises implanting n-type impurities utilizing an implant energy so as to provide second regions of n-type silicon carbide have a depth of from about 0.05 μm to about 1 μm.

70. The method of Claim 61, wherein the step of patterning an oxide layer comprises the step of thermally growing an oxide layer.

71. The method of Claim 70, wherein the step of thermally growing an oxide layer comprises thermally growing an oxide layer in an NO or an N_2O environment.

72. The method of Claim 70, wherein the step of thermally growing an oxide layer comprises the step of thermally growing an oxynitride layer.

73. The method of Claim 61, wherein the step of patterning an oxide layer comprises the step of forming an oxide-nitride-oxide (ONO) layer.

74. The method of Claim 61, further comprising the step of annealing the oxide layer in at least one of an NO environment or an N_2O environment.

75. The method of Claim 74, wherein the step of annealing provides an interface state density of an interface between the oxide layer and the drift layer, the first regions of n-type silicon carbide and the second regions of n-type silicon carbide of less than about 10^{12} $eV^{-1}cm^{-2}$ within from about 0.3 to about 0.4 eV of the conduction band energy of 4H polytype silicon carbide.

76. The method of Claim 61, wherein the step of annealing is preceded by the steps of:

patterning a fourth mask, the fourth mask being on the layer of n-type silicon carbide and the first regions of p-type silicon carbide and having opening therein corresponding to second regions of p-type silicon carbide disposed in respective ones of the first regions of p-type silicon carbide the second regions of silicon carbide

being adjacent the first regions of n-type silicon carbide and opposite the second regions of n-type silicon carbide; and

implanting p-type impurities utilizing the fourth mask so that the second regions of p-type silicon carbide have a carrier concentration greater than the carrier concentration of the first regions of silicon carbide.

77. The method of Claim 76, further comprising:

forming windows in the epitaxial layer positioned to expose the second regions of p-type silicon carbide; and

forming contacts within the window on the second regions of p-type silicon carbide and the first regions of n-type silicon carbide.

78. The method of Claim 61, further comprising forming a gate contact on the gate oxide layer.

79. The method of Claim 78, wherein step of forming a gate contact comprises the step of patterning p-type polysilicon so as to provide a gate contact on the gate oxide layer.

80. The method of Claim 61, wherein the first mask has openings which are spaced apart by a distance of from about 1 μm to about 10 μm.

81. The method of Claim 61, further comprising:

implanting n-type impurities into a face of the layer of n-type silicon carbide opposite the oxide layer so as to provide a second layer of n-type silicon carbide having a carrier concentration greater than the carrier concentration of the layer of n-type silicon carbide; and

forming a drain contact on the second layer of n-type silicon carbide.

82. The method of Claim 61, wherein the layer of n-type silicon carbide comprises a silicon carbide substrate.

83. A silicon carbide metal-oxide semiconductor field effect transistor, comprising:

a silicon carbide MOSFET, having an n-type silicon carbide drift layer, spaced apart p-type silicon carbide regions in the n-type silicon carbide drift layer and having n-type silicon carbide regions therein, and a nitrided oxide layer on the n-type silicon carbide drift layer; and

a region between the n-type silicon carbide regions and the drift layer and is adjacent the nitrided oxide layer that is configured to self deplet upon application of a zero gate bias.

43

~~84~~. A silicon carbide metal-oxide semiconductor field effect transistor according to Claim 42 ~~83~~, wherein the p-type silicon carbide regions comprise spaced apart regions of silicon carbide having aluminum implanted therein.

44

~~85~~. A silicon carbide metal-oxide semiconductor field effect transistor according to Claim 42 ~~83~~, wherein the region that is configured to self-deplete extends to but not into the n-type silicon carbide drift layer.

45

~~86~~. A silicon carbide metal-oxide semiconductor field effect transistor according to Claim 43 ~~83~~, further comprising an epitaxial layer of silicon carbide on the n-type silicon carbide drift layer between the p-type regions.

46

~~87~~. A silicon carbide metal-oxide semiconductor field effect transistor according to Claim 42 ~~83~~, wherein the region that is configured to self-deplete comprises a region of silicon carbide having a sheet charge corresponding to a sheet charge of an epitaxial layer of silicon carbide having a thickness of about 3500 Å and carrier concentration of about 2×10^{16} cm^{-3}.

47

~~88~~. A silicon carbide metal-oxide semiconductor field effect transistor according to Claim 42 ~~83~~, further comprising a gate contact on the oxide layer, the gate contact comprising p-type polysilicon.

48

~~89~~. A silicon carbide metal-oxide field effect transistor according to Claim 42 ~~83~~, wherein the silicon carbide comprises 4H polytype silicon carbide and wherein an interface between the oxide layer and the n-type drift layer has an interface state

density of less than 10^{12} $eV^{-1}cm^{-2}$ for energy levels between about 0.3 and about 0.4 eV of a conduction band energy of 4H polytype silicon carbide.

add 2